Applications of On-Chip Samplers for Test and Measurement of Integrated Circuits

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Introduction

Displaying the real-time behavior of critical signals on VLSI chips is difficult and can require expensive test equipment. We present a simple sampling technique to display the analog waveforms of high bandwidth on-chip signals on a laboratory oscilloscope. It is based on the subsampling of periodic signals as proposed in [1]. This circuit was used to verify the operation of a recent low-power SRAM design [2].

Sampling circuit

The idea behind the sampling technique is to exploit the high bandwidth of MOS transmission gates by using one to sample the analog voltage on a capacitor. This voltage is then converted to a current and driven off-chip. By making the internal waveform repetitive and then sampling only once per period, we can allow the bandwidth of the output current to be significantly lower than that of the internal signal being measured.

A complete measurement circuit consists of a number of samplers whose outputs are multiplexed into a single current mirror (Figure 1). M1-5 make up the voltage sampler and voltage-to-current converter. A periodic signal of period T is sampled by M1-2 using an externally generated clock which runs at a slightly different period T+Δt. M1 and M2 form a master/slave sample-and-hold circuit. A sequence of samples of the signal waveform at intervals of Δt is taken over a period of T/Δt cycles. Thus the sampler output is a time-expanded version of the signal waveform whose frequency is the beat frequency of the signal and sampling clock frequencies. PMOS M4 converts the sampled voltage into a current which is then mirrored twice and driven off-chip.

Without a gain stage between master and slave as in [1], charge sharing between C1 and C2 leads to a low-pass filtering of the sampled voltage. The bandwidth of this filter is set by the ratio C2/(C1+C2) and the sample spacing Δt. Our design has a capacitance ratio of 15fF/22.4fF = 0.67 and with a sample spacing of 7pS we obtain a theoretical bandwidth of 35GHz, although jitter in Δt will reduce this. The sampler's front end RC bandwidth of M1-C1 is ~5GHz.

The transconductance of each sampler is calibrated by sampling an externally supplied DC voltage through M3. The calibration results for 3 such samplers are shown in Figure 2. Note that variations between samplers require individual calibrations for accurate amplitude measurements. Clock feedthrough from M1-3 shows up as high frequency noise and is filtered out by an external low-pass filter. M5 is used to disable the sampler, allowing for sharing of a single output pin among all the samplers. The small sizes of M1-5 allow for a compact layout, and the extra loading of the sampler on the signal node is only 9.8fF. M1-5 require only 55μm^2 of area. The NMOS current mirrors and some control logic take another 320μm^2, and the PMOS current mirror 820μm^2.

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In the SRAM design, the chip core used a 1.0V supply. A separate boosted supply of 1.8V was used for driving M1-M5 and allowed measurement of full-swing core signals.

This design differs from that in [1] to make it more suitable for measuring on-chip waveforms. First, per-sampler calibration ports avoid process skew inaccuracies across samplers. Second, using an external source for the sampler clock instead of an on-chip delay line allows for a wide range of chip frequencies. Third, sharing the mirrors between samplers allows for very compact layout and a small pin overhead for the 18 samplers on the chip.

SRAM Measurements

The sampler output was fed into an oscilloscope, which was interfaced to a workstation for capturing, calibrating, and plotting results. A second sampler, placed on the chip clock, generated a clock at the beat frequency $\Delta t/T^2$, which was used to trigger the oscilloscope. This provided a timing reference for delay measurements of the sampled signals.

The SRAM is a low-power self-timed pulsed design described in [2]. High capacitance internal nodes such as predecode and write buses have half-Vdd amplitude. The bitline swings during reads are even smaller (a few hundred millivolts) and the read databus is a pulsed small swing bus.The probed waveforms of a 1.3V clock, the predecode lines, global wordlines, bitlines, sense enable, and read databus are shown in Figure 3 for a 1.0V core supply. Of these signals, only the clock and sense enable swing full-rail. The read databus is differential, but only one line is shown. The delay between the core clock rising edge and the read databus separation is measured to be 6.6 nS, compared with the simulated worst-case delay of 7 nS. We can see close matching between simulated and measured bitline waveforms in Figure 4. The senseamp kick-back during bitline precharge is also observed as a small kink in the bitline waveform.

Noise was a design concern because of the small swings and fairly long wires in the SRAM, and strategies such as bus braiding on the 8-bit predecode bus were used. This equalized the coupling from any one wire to the other seven. Using the samplers, we saw inter-wire coupling noise of ±40 mV on one wire in the predecode bus when an adjacent wire carried a 0.5V pulse (Figure 5). The wires are 1mm long with 0.45μm width and 0.6μm spacing.

Summary

We present applications of an on-chip sampling technique that allows for non-invasive measurements of analog waveforms of critical signals. This technique requires relatively inexpensive laboratory equipment, and increases the capacitive loading of the measured nodes by only a few fF. True on-chip bitline swings, clock waveforms, half-swing pulses, and noise couplings were observed on a low-power SRAM design.

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References

[1] P. Larsson and C. Svensson, "Measuring high-bandwidth signals in CMOS circuits," *Electronics Letters*, Vol. 29, No. 20, pp. 1761-2, September 1993.

[2] T. Mori et. al., "A 1V 0.9mW at 100MHz 2kx16b SRAM utilizing a Half-Swing Pulsed-Decoder and Write-Bus Architecture in 0.25μm Dual-V_t CMOS," to appear in *IEEE ISSCC Dig. Tech. Papers*, 1998

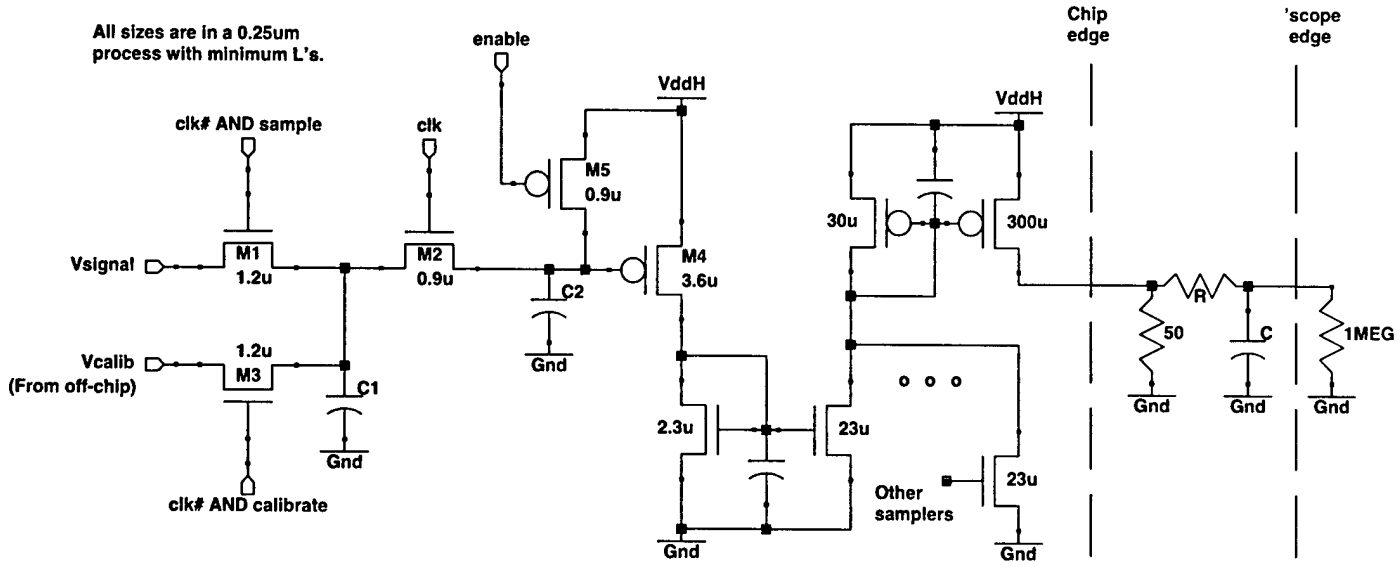

Figure 1: Sampler architecture

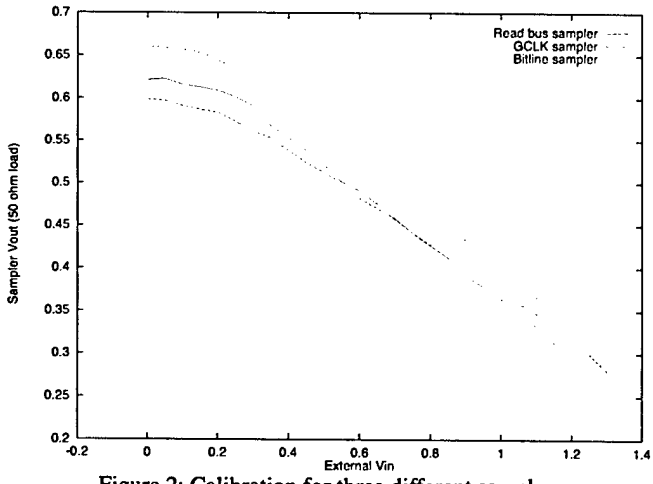

Figure 2: Calibration for three different samplers

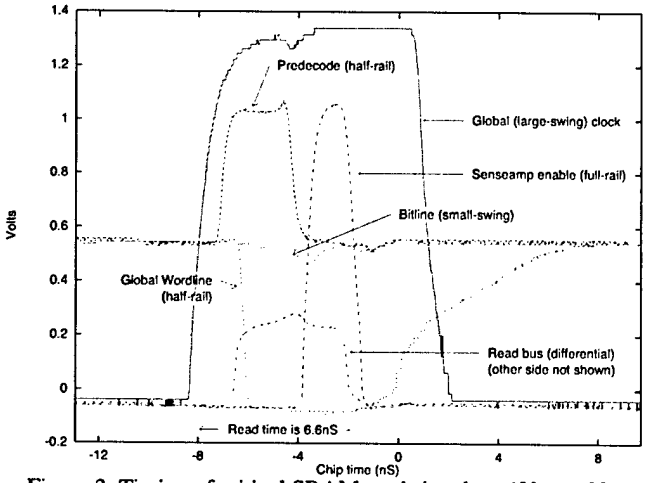

Figure 3: Timing of critical SRAM read signals at 1V core Vdd

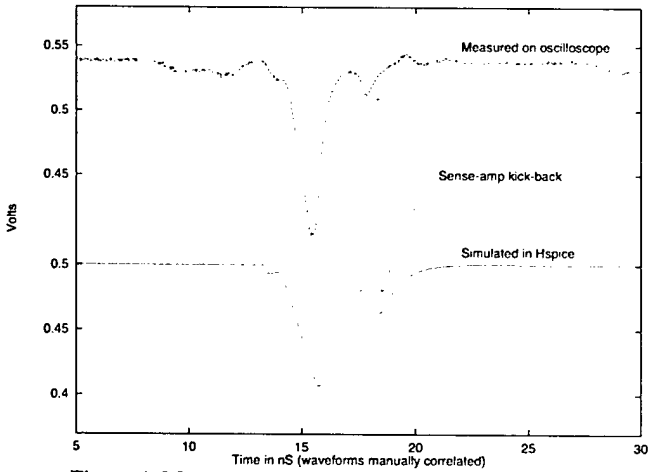

Figure 4: Measured and simulated bitlines (reading a 0)

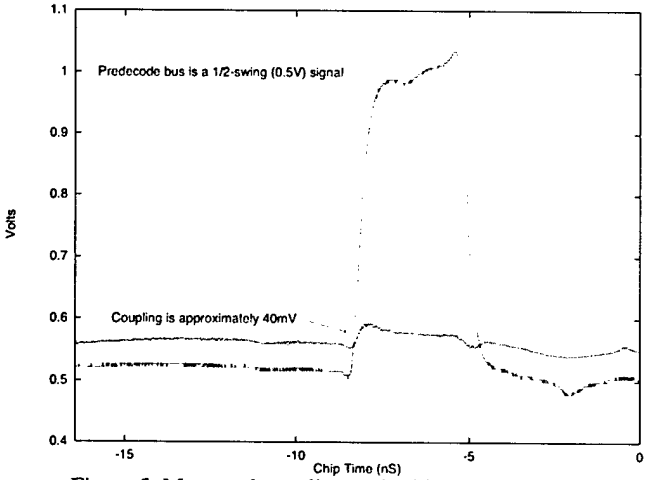

Figure 5: Measured coupling on braided predecode bus

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